WHAT IS CLAIMED IS:

1. A method for forming first and second linear structures of a first composition, said first and second linear structures meeting at right angles and being separated by a gap, said method comprising the steps of:

providing an etchable crystalline layer having said first composition;

growing first and second self-aligned nanowires of a second composition on a surface of said etchable crystalline layer, said first nanowire growing at right angles to said second nanowire, said first nanowire being separated from said second nanowire by a gap of less than 10 nm; and

anisotropically etching portions of said etchable layer that are not under said first and second nanowires using said first and second nanowires as a mask, to form said first and second linear structures of said first composition.

2. The method of Claim 1 wherein said etchable layer has an insulating layer beneath said layer and wherein said step of anisotropically etching portions of said etchable layer removes material of said first composition down to said insulating layer.

3. The method of Claim 1 wherein said step of growing said first and second self-aligned nanowires comprises depositing material of said second composition on said surface and wherein said material of said second composition forms crystals on said surface that have an asymmetric lattice mismatch with respect to said crystalline surface.

4. The method of Claim 3 wherein said lattice mismatch is less than 4 percent in the directions that are parallel to the direction in which said linear nanowires and greater than 4 percent in all other directions on said surface.

5. The method of Claim 1 wherein said first composition comprises silicon and wherein said second composition comprises a metal silicide of the chemical formula MSi_2, where M is a metal selected from the group consisting of Sc, Y, and the rare earths.

6. The method of Claim 5 wherein the rare earth is chosen from the group consisting of Er, Dy, Gd, Th, Ho, Tb, and Sm.

7. The method of Claim 1 wherein said first composition comprises a semiconductor chosen from the group consisting of Si, Ge, Ge_xSi_{1-x} where $0 < x < 1$, GaAs, InAs, AlGaAs, InGaAs, AlGaAs, GaN, InN, AlN, AlGaN, and InGaN.

8. The method of Claim 1 wherein said first composition comprises a metal chosen form the group consisting of Al, Cu, Ti, Cr, Fe, Co, Ni, Zn, Ga, Nb, Mo, Pd, Ag, In, Ta, W, Re, Os, Ir, Pt, and Au, and alloys thereof.

9. The method of Claim 1 wherein said step of growing said first and second self-aligned nanowires comprises depositing an island of a seed material at a location that determines the location of said first self-aligned nanowire.

10. The method of Claim 9 wherein said island is less than 10 nm in width.

11. The method of Claim 1 wherein said second composition comprises a metal silicide of the chemical formula MSi_2, and wherein said seed material comprises the element M.

12. An electric device comprising:

a first elongated nanowire on an insulating surface and a second elongated nanowire on said insulating surface at right angles to said first elongated nanowire and separated therefrom by a gap of between 0.4 nm and 10 nm.

13. The electric device of Claim 12 wherein said first and second nanowires form a transistor having a source, drain, and gate, and wherein said first nanowire has first and second ends;

said first end of said first nanowire forming said source, said second end of said first nanowire forming said drain, and said second nanowire forming said gate.

14. The electrical device of Claim 12 wherein said first elongated nanowire comprises a semiconductor chosen from the group consisting of Si, Ge, Ge_xSi_{1-x} where $0 < x < 1$, GaAs, InAs, AlGaAs, InGaAs, AlGaAs, GaN, InN, AlN, AlGaN, and InGaN.

15. The electrical device of Claim 12 wherein said gap is filled with a material that stores electrical charge .

16. The electrical device of Claim 12 wherein said gap is filled with a material having electric dipole moment.

17. The electrical device of Claim 12 wherein said first and second nanowires form a two-electrode memory switching device, said first nanowire firming the first electrode of said switching device and said second nanowire forming the second electrode of said switching device.